

(11) Publication number:

07007838 A

Generated Document.

PATENT ABSTRACTS OF JAPAN

(21) Application number: 05144787

(51) Intl. Cl.: H02H 3/00

(22) Application date: 16.06.93

(30) Priority:

(43) Date of application publication:

10.01.95

(84) Designated contracting states:

(72) Inventor: FURUKAWA KATSUHIRO

(71) Applicant: TOSHIBA CORP

(74) Representative:

(54) CONTROLLER FOR CIRCUIT BREAKER

(57) Abstract:

level adjusting work and reducing the elements by performing over current manufacturing cost of the controller PURPOSE: To simplify the circuit protecting operations requiring an number of required analog circuit by eliminating the need of output circuit breakers and suppress the configuration of a controller for nverse time lag characteristic 18/03/2005

through digital operation.

CONSTITUTION: An A/D converter corresponding to the magnitude of the phase load current value indicated by he effective values. When the MC 37 detects the presence of a fault current digital voltage signals, and inputs the values of the maximum load currents trigger pulse after performing inverse indicated by the digital signals based arithmetic operation on the effective from the level-discriminated results, maximum load currents out of those urns on a thyristor 38 and causes a digital signals to a microcomputer 36 samples analog voltage signals from burden circuits 29a and 29c, on a preset program and executes ripping device 39 to open a main circuit contact 22 by outputting a converts the sampled signals into (MC) 37. The MC 37 selects the and level discrimination on each time lagging operations fault current.

COPYRIGHT: (C)1995, JPO

18/03/2005

18/03/2005